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TITLE: Microprocessor and data flow microprocessor having vector operation function

Detailed Description Paragraph Right (102):
In FIG. 22, the arrow extending from "C" to the rectangular block is the latch control signal, and this rectangular block is the data latch. The content to be latched may include address, tag and data. The address is the hash address for accessing the hash memory, and it is composed of color/generation and the destination node number of input packet. The tag information of the input packet is inputted to the tag, and the operand information is inputted to the data. The left operand is fed to the upper path of the data, and the right operand, to the lower path.

Detailed Description Paragraph Right (359):
As the method of composing matching memory unit MM, the parallel hash method is general. However, in the event of hash conflict, it is necessary to access the memory sequentially according to the pointer chain, and multiple hash conflicts occur on a same address, it means a major penalty to sacrifice time. This processor, to solve this problem, uses both hash memory and associative memory. The packet undergoing hash conflict is stored in the associative memory, and by searching the both memories for the input packet, it is possible to process matching at a certain delay, regardless of presence or absence of hash conflict.